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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,547	04/02/2004	Heonchul Park	REDPINE - CODEBOOT	2537

24346 7590 05/28/2008

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EXAMINER	
LINDSEY, MATTHEW S	

ART UNIT	PAPER NUMBER
2151	

MAIL DATE	DELIVERY MODE
05/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,547	PARK, HEONCHUL	
	Examiner	Art Unit	
	MATTHEW S. LINDSEY	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending in this application. Claims 1, 10, 11 and 12 are amended as filed on 26 March 2008. Claims 20-23 are canceled as filed on 26 March 2008. Claim 24 is newly presented, as filed on 26 March 2008.

Claim Objections

2. Claim 10 is objected to because of the following informalities: the claim recites the limitation "using instructions placed in said memory by said third step" (pg 11, lines 6-7). Said third step recites: "a CPU executing said instructions placed into memory by said second step" (pg 11, lines 3-4), and the second step recites: "said DMA controller copying instructions from said ROM referenced by said value a memory location referenced by said DST value" (pgs 10-11, lines 22-23, and 1-2). Said second step places instructions in said memory, said third step executes said instructions, so the limitation "using instructions placed in memory by said third step" (pg 11, lines 6-7) appears to be a typo.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5-7, 10, 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaChance (US 7,017,038) in view of Baltz (US 6,058,474), and further in view of Chang (US 2003/0126242).

5. With respect to Claim 1, LaChance discloses: "An apparatus for the downloading of a code image (Abstract, lines 10-13), said apparatus having:

a Sequence Controller generating a ROM controller output (Col. 4, lines 64-67 and Col. 5, lines 1-2, where the device select signals for the boot FLASH are generated by the bus multiplexer) and a CPU enable output (Col. 6, lines 25-27, specifically CPU startup);

a ROM having a boot image (Col. 3, lines 30-32);

a DMA controller (Col. 4, lines 49-50)",

"a ROM controller coupled to said ROM (Figure 3, object 74)", and

"a CPU coupled to and executing instructions from said memory (Col. 3, lines 11-13, and Col. 4, lines 18-20, where the CPU begins executing after the operating

system has been loaded into memory), said CPU enabled upon the assertion of said CPU enable output (Col. 6, lines 25-27, specifically CPU startup)".

LaChance does not disclose: the ROM "having a SRC value, a DST value, a LENGTH value",

the DMA controller "having a SRC register specifying a source location, a DST register specifying a destination location, and a LENGTH register, said DMA controller moving an amount of data specified by said LENGTH register from said source location to said destination location",

"said ROM controller initializing said DMA controller upon assertion of said ROM controller enable output by copying said SRC value from said ROM to said DMA controller SRC register, said DST value from said ROM to said DMA controller DST register, and said LENGTH value from said ROM to said DMA controller LENGTH register",

"a memory coupled to said DMA controller, said DMA controller copying at least a part of said boot image from said ROM into said memory prior to the assertion of said CPU enable output",

"a wireless receiver", "a wireless front end coupled to said CPU", or "from a source coupled to a wireless link accessed through said wireless front end".

However, Baltz discloses: the ROM "having a SRC value (Col. 6, lines 64-67), a DST value (Col. 7, lines 12-15), a LENGTH value (Col. 7, lines 3-11)",

the DMA controller "having a SRC register specifying a source location (Col. 6, lines 47-49, source address generator provides a source address), a DST register specifying a destination location (Col. 6, lines 49-51, where destination address generator provides a destination address), and a LENGTH register (Col. 7, lines 3-11, where the amount of data is loaded into a counter), said DMA controller moving an amount of data specified by said LENGTH register (Col. 7, lines 3-11, where the amount of data to be transferred is loaded into a counter) from said source location (Col. 6, lines 47-49) to said destination location (Col. 6, lines 49-51)",

"said ROM controller (Col. 6, lines 51-54, where initialization circuitry is ROM controller) initializing said DMA controller (Col. 6, lines 1-4) upon assertion of said ROM controller enable output by copying said SRC value from said ROM to said DMA controller SRC register (Col. 6, lines 64 – Col. 7, line 2, where source address generator is loaded with a source address when the reset signal transitions), said DST value from said ROM to said DMA controller DST register (Col. 7, lines 12-15, where destination address generator is set to start at a destination address when reset signal transitions), and said LENGTH value from said ROM to said DMA controller LENGTH register (Col. 7, lines 3-11, where the amount of data, or length, to be transferred is loaded into counter 231 when reset signal transitions)",

"a memory coupled to said DMA controller, said DMA controller copying at least a part of said boot image from said ROM into said memory prior to the assertion of said CPU enable output (Col. 4, lines 42-44, where the DMA controller is initialized to perform a boot load, and Col. 4, lines 53-56, where during the boot load process CPU

reset signal is held asserted, so that no instruction processing is performed by the CPU)",

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance with the teachings of Baltz to include support for a ROM having SRC, DST, and LENGTH values, a ROM controller for enabling a DMA controller, and copying at least a part of boot image from ROM into memory prior to CPU enablement. Motivation to combine these references comes from Baltz where: "After the DMA transfer is complete, CPU control circuitry causes the CPU to start execution of the program at a predetermined location in internal memory. Because of this novel program loading mechanism, a boot ROM is not required within the microprocessor" (Col. 1, lines 60-65). Therefore by combining the references, a microprocessor can save memory space by not having a boot ROM within the microprocessor.

The combination of LaChance and Baltz does not disclose: "a wireless receiver", "a wireless front end coupled to said CPU", or "from a source coupled to a wireless link accessed through said wireless front end".

However Chang discloses: "a wireless receiver ([0016], lines 1-4, "wireless devices" require a wireless receiver to function)" and "a wireless front end coupled to said CPU ([0016], lines 1-4, wireless devices contain a wireless front end coupled to a CPU)", and "from a source coupled to a wireless link accessed through said wireless

front end ([0018], lines 1-7, where wireless devices are communicatively linked to the storage communications network)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teachings of LaChance and Baltz with the teachings of Chang to include wireless network support. Motivation to combine these comes from Chang, "The present invention is directed towards a network boot system and method that reduces or even eliminates the need for local storage at local boot clients (e.g., servers, desktop computers, laptop, or wireless devices, and the like) ([0016], lines 1-4)". Therefore by combining the booting system of LaChance and Baltz with the teachings of Chang to include wireless network support, client devices can boot wirelessly with little or no need for local storage.

6. With respect to Claim 3, the combination of LaChance, Baltz, and Chang disclose: "The apparatus of Claim 1 where said memory is a dynamic random access memory (LaChance, Col. 4, lines 43-44, "the main memory 60 is implemented as a 256 Mbyte SDRAM", SDRAM is a synchronous access form of DRAM)".

7. With respect to Claim 5, the combination of LaChance, Baltz, and Chang disclose: "The apparatus of Claim 3 where said CPU downloads said operating system image into said dynamic random access memory (LaChance, Col. 4, lines 11-15)".

8. With respect to Claim 6, the combination of LaChance, Baltz, and Chang disclose: "The apparatus of Claim 1 where said sequence controller uniquely asserts said ROM controller output and said CPU enable output (LaChance, Col. 4, lines 18-20, "after the copy of the CPU operating system code 20 is loaded into main memory 16, the CPU begins its execution", after the copy is done there is inherently a signal that tells the CPU to start executing, this signal being asserted at a different time than the ROM controller output, which happens before loading the operating system code into main memory)".

9. With respect to Claim 7, the combination of LaChance, Baltz, and Chang disclose: "The apparatus of Claim 1 first asserts said ROM controller output, and asserts said CPU enable output after completion of copying of said LENGTH from said SRC to said DST (LaChance, Col. 4, lines 18-20, where the ROM controller output is asserted before loading the operating system code into main memory and the CPU starts execution after the operating system code is loaded into main memory, thereby assertion of the ROM controller output happens first, and assertion of a CPU enable, the CPU begins its execution, happens after loading the operating system into memory)".

10. With respect to Claim 10, LaChance discloses: "a third step of a CPU executing said instructions located in a memory (Col. 4, lines 18-20);

a fourth step of said CPU downloading an operating system program from a remote host (Col. 4, lines 11-14) using instructions placed in memory by said third step, thereafter executing said operating system program (Col. 4, lines 18-20)".

LaChance does not disclose: "A process for the downloading of code to a wireless receiver said process comprising: a first step of copying a SRC value, a DST value, and a LENGTH value from a ROM to a DMA controller;

a second step of said DMA controller copying instructions from said ROM referenced by said SRC value to a memory location referenced by said DST value".

However, Baltz discloses: "a first step of copying a SRC value (Col. 6, lines 64-66), a DST value (Col. 7, lines 12-15), and a LENGTH value (Col. 7, lines 3-11) from a ROM to a DMA controller (Col. 6, lines 64 - Col. 7, lines 15, where the source address generator of the DMA controller is loaded with a source address, a destination address generator is set to a start address, and the amount of data to be transferred is loaded into a counter when the reset signal transitions);

a second step of said DMA controller copying instructions from said ROM referenced by said SRC value (Col. 6, lines 47-49) to a memory location referenced by said DST value (Col. 6, lines 49-51)"

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance with the teachings of Baltz to include specific details of DMA controller operation. LaChance discloses a DMA controller (Col. 4, lines 49-50) but does not go into details about its operation. Baltz

discloses the operations of a DMA controller (Col. 6, lines 43 - Col. 7 lines 22). Therefore by combining the booting system of LaChance with the DMA controller details disclosed in Baltz, one can use a DMA controller to transfer data between main memory and peripheral device, or between peripheral devices without intervention of the host processor.

The combination of LaChance and Baltz does not disclose: "A process for the downloading of code to a wireless receiver".

However Chang discloses: "A process for the downloading of wireless code to a receiver ([0007], Col. 2, lines 6-8, and [0016], lines 1-4, "wireless devices" require a wireless receiver to function)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz with the teachings of Chang to include wireless network support. Motivation to combine these comes from Chang, "The present invention is directed towards a network boot system and method that reduces or even eliminates the need for local storage at local boot clients (e.g., servers, desktop computers, laptop, or wireless devices, and the like) ([0016], lines 1-4)". Therefore by combining the booting system of LaChance in view of Baltz with the teachings of Chang to include wireless network support, client devices can boot wirelessly with little or no need for local storage.

11. With respect to Claim 12, the combination of LaChance, Baltz and Chang discloses: "The process of Claim 10, where said DST value causes said DMA controller to write to a region in said memory (Baltz, Col. 6, lines 49-51)"

12. With respect to Claim 24, LaChance discloses: "An apparatus for the downloading of a code image (Abstract, lines 10-13), said apparatus having:

a Sequence Controller generating a ROM controller output (Col. 4, lines 64-67 and Col. 5, lines 1-2, where the device select signals for the boot FLASH are generated by the bus multiplexer) and a CPU enable output (Col. 6, lines 25-27, specifically CPU startup);

a ROM having a boot image (Col. 3, lines 30-32);

a DMA controller (Col. 4, lines 49-50)",

"a ROM controller coupled to said ROM (Figure 3, object 74)", and

"a CPU coupled to and executing instructions from said memory (Col. 3, lines 11-13, and Col. 4, lines 18-20, where the CPU begins executing after the operating system has been loaded into memory), said CPU enabled upon the assertion of said CPU enable output (Col. 6, lines 25-27, specifically CPU startup)",

"a CPU coupled to said memory (Col. 3, lines 11-13), said CPU enabled upon the assertion of said CPU enable output (Col. 6, lines 25-27, specifically CPU startup)", and "said CPU thereafter executing said boot image from said memory (Col. 4, lines 18-20, where the CPU begins executing after the operating system has been loaded into memory)".

LaChance does not disclose: the ROM "having a SRC value, a DST value, a LENGTH value",

the DMA controller "having a SRC register specifying a source location, a DST register specifying a destination location, and a LENGTH register, said DMA controller moving an amount of data specified by said LENGTH register from said source location to said destination location",

"said ROM controller initializing said DMA controller upon assertion of said ROM controller enable output by copying said SRC value from said ROM to said DMA controller SRC register, said DST value from said ROM to said DMA controller DST register, and said LENGTH value from said ROM to said DMA controller LENGTH register",

"a memory coupled to said DMA controller, said DMA controller copying at least a part of said boot image from said ROM into said memory",

"said CPU enable output asserted after said DMA controller has moved said boot image from said ROM into said memory", or

"a wireless receiver".

However, Baltz discloses: the ROM "having a SRC value (Col. 6, lines 64-67), a DST value (Col. 7, lines 12-15), a LENGTH value (Col. 7, lines 3-11)",

the DMA controller "having a SRC register specifying a source location (Col. 6, lines 47-49, source address generator provides a source address), a DST register

specifying a destination location (Col. 6, lines 49-51, where destination address generator provides a destination address), and a LENGTH register (Col. 7, lines 3-11, where the amount of data is loaded into a counter), said DMA controller moving an amount of data specified by said LENGTH register (Col. 7, lines 3-11, where the amount of data to be transferred is loaded into a counter) from said source location (Col. 6, lines 47-49) to said destination location (Col. 6, lines 49-51)",

"said ROM controller (Col. 6, lines 51-54, where initialization circuitry is ROM controller) initializing said DMA controller (Col. 6, lines 1-4) upon assertion of said ROM controller enable output by copying said SRC value from said ROM to said DMA controller SRC register (Col. 6, lines 64 – Col. 7, line 2, where source address generator is loaded with a source address when the reset signal transitions), said DST value from said ROM to said DMA controller DST register (Col. 7, lines 12-15, where destination address generator is set to start at a destination address when reset signal transitions), and said LENGTH value from said ROM to said DMA controller LENGTH register (Col. 7, lines 3-11, where the amount of data, or length, to be transferred is loaded into counter 231 when reset signal transitions)",

"a memory coupled to said DMA controller, said DMA controller copying at least a part of said boot image from said ROM into said memory (Col. 4, lines 42-44, where the DMA controller is initialized to perform a boot load)", and

"said CPU enable output asserted after said DMA controller has moved said boot image from said ROM into said memory (Col. 4, lines 53-56, where the CPU reset

signal is held asserted during the DMA operation, so that no instruction processing is performed by the CPU)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance with the teachings of Baltz to include support for a ROM having SRC, DST, and LENGTH values, a ROM controller for enabling a DMA controller, and copying at least a part of boot image from ROM into memory prior to CPU enablement. Motivation to combine these references comes from Baltz where: "After the DMA transfer is complete, CPU control circuitry causes the CPU to start execution of the program at a predetermined location in internal memory. Because of this novel program loading mechanism, a boot ROM is not required within the microprocessor" (Col. 1, lines 60-65). Therefore by combining the references, a microprocessor can save memory space by not having a boot ROM within the microprocessor.

The combination of LaChance and Baltz does not disclose: "a wireless receiver".

However Chang discloses: "a wireless receiver ([0016], lines 1-4, "wireless devices" require a wireless receiver to function)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teachings of LaChance and Baltz with the teachings of Chang to include wireless network support. Motivation to combine these comes from Chang, "The present invention is directed towards a network boot system and method that reduces or even eliminates the need for local storage at local boot clients (e.g.,

servers, desktop computers, laptop, or wireless devices, and the like) ([0016], lines 1-4)". Therefore by combining the booting system of LaChance and Baltz with the teachings of Chang to include wireless network support, client devices can boot wirelessly with little or no need for local storage.

13. Claims 2, 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaChance in view of Baltz and Chang as applied to claims 1 and 10 above, and further in view of Bashford et al. (US 6,529,989 B1).

14. With respect to Claim 2, the combination of LaChance, Baltz and Chang do not disclose: "where said memory is a static random access memory".

However Bashford discloses: "where said memory is a static random access memory (Col. 5, lines 10-13)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang with the teachings of Bashford to include using SRAM. Motivation for combining these references comes from the properties of SRAM, specifically the contents of the SRAM are valid as long as power is applied, as opposed to DRAM where the contents need to be periodically refreshed. Therefore by modifying the booting system of LaChance in view of Baltz and Chang, with the teachings of Bashford to include SRAM, the booting system does not need to periodically refresh the memory in order to retain valid data as long as power is applied.

15. With respect to Claim 4, the combination of LaChance, Baltz, Chang, and Bashford disclose: "The apparatus of claim 2 where said static random access memory is addressed by said SRC register (Baltz, Col. 6, lines 49-51)"

16. With respect to Claim 11, the combination of LaChance, Baltz and Chang disclose: "The process of Claim 10 where said SRC value causes said DMA controller to read from a region in said ROM (Baltz, Col. 6, lines 49-51)".

The combination of LaChance, Baltz and Chang do not disclose "said LENGTH defines a contiguous region of said ROM".

However Bashford discloses: "and said LENGTH defines a contiguous region of said ROM (Col. 6, lines 42-44)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang with the teachings of Bashford to include contiguous storage in ROM. Motivation for combining these references comes from simplification of the boot up process. By storing data in the ROM in a contiguous region there is no need to read from many disjointed parts of the ROM. By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Bashford to include using a contiguous region of the ROM, the booting system becomes less complex.

17. Claims 8-9, 13-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaChance in view of Baltz and Chang as applied to claims 1 and 10 above, and further in view of Wiedeman et al. (US 6,985,454 B1).

18. With respect to Claim 8, the combination of LaChance, Baltz and Chang disclose: "where said boot image includes instructions for: sending a download request (LaChance, Col. 2, lines 15-18)".

The combination of LaChance, Baltz and Chang do not disclose "receiving a packet accompanied by a sequence number; discarding a packet with the same sequence number as an earlier-received packet; accepting a packet with a unique sequence number; sending a download request if a gap in sequence numbers is detected".

However Wiedeman discloses: "receiving a packet accompanied by a sequence number (Figure 9, the TCP header contains a sequence number, and Col 9, lines 46-48); discarding a packet with the same sequence number as an earlier-received packet (Figure 15B, and Col. 12, lines 1-5); accepting a packet with a unique sequence number (Figure 15B and Col. 12, lines 1-5); sending a download request if a gap in sequence numbers is detected (Col. 12, lines 17-21, specifically in the presence of a specific non-acknowledgement)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang to include the teachings of Wiedeman to include a specific network protocol for sending

redundant packets. Motivation to combine these comes from Wiedeman, where it is disclosed that by sending multiple packets "provides robustness in that it is less likely a given packet will be lost, thereby requiring fewer re-transmissions" (Col 21, lines 3-6). By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman it becomes less likely a packet will be lost during transmission.

19. With respect to Claim 9, the combination of LaChance, Baltz and Chang disclose: "The apparatus of claim 1 where a download server (Chang, [0017], lines 6-11) with a wireless interface receives a download request from a wireless client (Chang, [0016], lines 1-4, specifically wireless devices) and responds to said download request (Chang, [0017], lines 10-11, where the server responds to the request because the operating system is downloaded and the server controls access to the pooled storage which contains system boot images, where the boot images include a standard operating system [0012], lines 4-5)".

The combination of LaChance, Baltz and Chang do not disclose: "by: sending download data including a sequence number, each download data comprising an original packet and a duplicate packet each including said sequence number; incrementing the sequence number for each subsequently sent download data; upon sending all said download data, thereafter sending a "done" packet indicating completion of the download".

However Wiedeman discloses: "by: sending download data including a sequence number (Figure 9, the TCP header contains a sequence number, and Col 9, lines 46-

48), each download data comprising an original packet and a duplicate packet each including said sequence number (Col. 11, lines 41-46); incrementing the sequence number for each subsequently sent download data (It is well known in the art at the time of the invention that a TCP header sequence number is incremented in subsequent packets); upon sending all said download data, thereafter sending a "done" packet indicating completion of the download (Figure 9, the TCP header contains a FIN flag to indicate that the current packet is the last packet in the current message)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman to include a specific network protocol for sending duplicate packets and a done packet. Motivation to combine these comes from Wiedeman, where it is disclosed that by sending multiple packets "provides robustness in that it is less likely a given packet will be lost, thereby requiring fewer re-transmissions" (Col 21, lines 3-6). By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman it becomes less likely a packet will be lost during transmission.

20. With respect to Claim 13, the combination of LaChance, Baltz and Chang disclose: "The process of claim 10 where said third step said CPU instructions includes the instructions for: transmitting a download request (LaChance, Col. 2, lines 15-18)"

The combination of LaChance, Baltz and Chang does not disclose: "receiving a packet accompanied by a sequence number; discarding a packet with the same

sequence number as an earlier-received packet; accepting a packet with a unique sequence number; sending a download request if a gap in sequence numbers is detected".

However Wiedeman discloses "receiving a packet accompanied by a sequence number (Figure 9, the TCP header contains a sequence number, and Col 9, lines 46-48); discarding a packet with the same sequence number as an earlier-received packet (Figures 15B, and Col. 12, lines 1-5); accepting a packet with a unique sequence number (Figures 15B, and Col 12., lines 2-5); sending a download request if a gap in sequence numbers is detected (Col. 12, lines 17-21)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang to include the teachings of Wiedeman to include a specific network protocol for sending duplicate packets. Motivation to combine these comes from Wiedeman, where it is disclosed that sending redundant packets "provides robustness in that it is less likely a given packet will be lost, thereby requiring fewer re-transmissions" (Col 21, lines 3-6). By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman it becomes less likely a packet will be lost during transmission.

21. With respect to Claim 14, the combination of LaChance, Baltz and Chang disclose: "The process of claim 10 where said fourth step includes: sending a download request (LaChance, Col. 2, lines 15-18)".

However, the combination of LaChance, Baltz and Chang does not disclose: "receiving a packet accompanied by a sequence number; discarding a packet with the same sequence number as an earlier-received packet; accepting a packet with a unique sequence number; sending a download request if a gap in sequence numbers is detected".

However Wiedeman discloses: "receiving a packet accompanied by a sequence number (Figure 9, the TCP header contains a sequence number, and Col 9, lines 46-48); discarding a packet with the same sequence number as an earlier-received packet (Figures 15B, and Col. 12, lines 2-5); accepting a packet with a unique sequence number (Figures 15B, and Col 12., lines 2-5); sending a download request if a gap in sequence numbers is detected (Col. 12, lines 17-21)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang to include the teachings of Wiedeman to include a specific network protocol for sending duplicate packets. Motivation to combine these comes from Wiedeman, where it is disclosed that sending redundant packets "provides robustness in that it is less likely a given packet will be lost, thereby requiring fewer re-transmissions" (Col 21, lines 3-6). By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman it becomes less likely a packet will be lost during transmission.

22. With respect to Claim 15, the combination of LaChance, Baltz and Chang do not disclose: "where said remote host responds to said download request by: sending

download data including a sequence number, each download data comprising an original packet and a duplicate packet each including said sequence number; incrementing the sequence number for each subsequently sent download data; upon sending all said download data, thereafter sending a "done" packet indicating completion of the download".

However Wiedeman discloses: "where said remote host responds to said download request (It is inherent to function that the remote host will respond to download requests) by: sending download data including a sequence number (Figure 9, the TCP header contains a sequence number, and Col 9, lines 46-48), each download data comprising an original packet and a duplicate packet each including said sequence number (Col. 11, lines 41-46); incrementing the sequence number for each subsequently sent download data (It is well known in the art at the time of the invention that a TCP header sequence number is incremented in subsequent packets); upon sending all said download data, thereafter sending a "done" packet indicating completion of the download (Figure 9, the TCP header contains a FIN flag to indicate that the current packet is the last packet in the current message)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman to include a specific network protocol for sending duplicate packets and a done packet. Motivation to combine these comes from Wiedeman, where it is disclosed that sending redundant packets "provides robustness in that it is less likely a given packet will be lost, thereby requiring fewer re-transmissions" (Col 21,

lines 3-6). By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman it becomes less likely a packet will be lost during transmission.

23. With respect to Claim 16, the combination of LaChance, Baltz, Chang and Wiedeman disclose: "The process of claim 15 where said download data includes an operating system for use by said CPU (LaChance, Col. 2, lines 15-18)".

24. With respect to Claim 17, the combination of LaChance, Baltz and Chang do not disclose: "where said original and said duplicate packet are not interleaved".

However Wiedeman discloses: "where said original and said duplicate packet are not interleaved (Col. 11, lines 42-46, in this instance duplicate copies of the same packets are sent out at the same time and are thus not interleaved)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang to include the teachings of Wiedeman to include not interleaving the packets. Motivation for this modification comes from the art where it is well known that interleaving a message provides more latency during transfer. By modifying the booting system of LaChance in view of Baltz and Chang to include not interleaving the packets of Wiedeman therefore the transfer of data has less latency.

25. With respect to Claim 19, the combination of LaChance, Baltz and Chang does not disclose: "where said duplicate packet includes a plurality of packets, each said packet having the same said Tx_Seq_Num as said original packet".

However Wiedeman discloses: "where said duplicate packet includes a plurality of packets, each said packet having the same said Tx_Seq_Num as said original packet (Col. 11, lines 42-46, "by simply sending the same packet towards more than one satellite", the multiple same packets implicitly have the same sequence number, and Col. 12, lines 29-34 describes multiple redundant packets, 2' and 2")".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang to include the teachings of Wiedeman to include multiple duplicate packet transmission. Motivation to combine these comes from Wiedeman, where it is disclosed that by sending redundant packets "provides robustness in that it is less likely a given packet will be lost, thereby requiring fewer re-transmissions" (Col 21, lines 3-6). By modifying the booting system of LaChance in view of Baltz and Chang with the teachings of Wiedeman it becomes less likely a packet will be lost during transmission.

29. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over LaChance in view of Baltz and Chang as applied to claim 10 above, and further in view of Schuster et al. (US 6,170,075).

30. With respect to Claim 18, the combination of LaChance, Baltz and Chang does not disclose: "where said original and said duplicate packet are interleaved".

However Schuster discloses: "where said original and said duplicate packet are interleaved (Col. 12, lines 43-48)".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the booting system of LaChance in view of Baltz and Chang to include the teachings of Schuster to include interleaving packets. Motivation for this modification comes from Schuster, "This scheme may be enhanced to be more robust to burst errors by having network access server 18 interleave the originals and copies." (Col. 12, lines 43-45). By modifying the booting system of LaChance in view of Baltz and Chang to include the teachings of Schuster to include interleaving the original and copies, the booting system of LaChance in view of Baltz and Chang becomes more robust to burst errors.

Response to Arguments

26. Applicant's arguments, see pg 15, line 6 – pg 16, lines 6, filed 26 March 2008, with respect to Drawings have been fully considered and are persuasive. The objection of the drawings has been withdrawn.

27. Applicant's arguments, see pg 16, lines 10-22, filed 26 March 2008, with respect to Specification have been fully considered and are persuasive. The objection of the specification has been withdrawn.

28. Applicant's arguments, see pg 17, lines 1-4, filed 26 March 2008, with respect to Objection to Claim 1 have been fully considered and are persuasive. The objection of the specification has been withdrawn.

29. Applicant's arguments, see pg 17, line 6 - pg 19, line 4, filed 26 March 2008, with respect to the rejection(s) of claim(s) 1 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Baltz. Applicant argues: "These three values and a boot image are copied into memory, after which the CPU begins executing" (pg 17, lines 12-14), "The initialization of the DMA controller of claim 1 occurs before the CPU has a program loaded to execute" (pg 18, lines 3-4). Baltz discloses a DMA being initialized prior to the CPU, and transferring an amount of boot data from a source to a destination (Col. 4, lines 42 – 56, and Col. 6, line 43 – Col. 7, line 22). Specifically, Baltz discloses: "During this boot load process, CPU_Reset_signal 79 is held in an asserted state by DMA0 100 so that no instruction processing is performed by CPU 10" (Col. 4, lines 53-56).

30. Applicant's arguments, see pg 19, lines 6-8, filed 26 March 2008, with respect to the rejection(s) of claim(s) 3, 5, 6 and 7 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Baltz, see remarks above.

31. Applicant's arguments, see pg 19, line 10 - pg 20, line 3, filed 26 March 2008, with respect to the rejection(s) of claim(s) 10 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Baltz. Applicant argues: "Applicant notes that neither the initialization of the DMA controller by the ROM controller while the CPU is inactive in claim 10, first step, nor the movement of a boot image from the ROM to the memory while the CPU is inactive in claim 10 second step are found" (pg 19 line 20-pg 20 line 2). Baltz discloses a DMA being initialized prior to the CPU, and transferring an amount of boot data from a source to a destination (Col. 4, lines 42 – 56, and Col. 6, line 43 – Col. 7, line 22). Specifically, Baltz discloses: "During this boot load process, CPU_Reset_signal 79 is held in an asserted state by DMA0 100 so that no instruction processing is performed by CPU 10" (Col. 4, lines 53-56).

32. Applicant's arguments, see pg 20, lines 5-7, filed 26 March 2008, with respect to the rejection(s) of claim(s) 12 under 35 USC 103 have been fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Baltz, see remarks above.

33. Applicant's arguments, see pg 20, lines 9-12, filed 26 March 2008, with respect to the rejection(s) of claim(s) 2, 4, and 11 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Baltz, see remarks above.

34. Applicant's arguments, see pg 20 line 14 - pg 21, line 18, filed 26 March 2008, with respect to rejection of claims 8, 9, 13-15, 17, 18, and 19 have been fully considered but they are not persuasive. Applicant argues "each packet is instead sent a plurality of times in hope that at least one packet from each set of identical duplicates will be correctly received" (pg 21, lines 2-5). Wiedman discloses: "In general multiple packets can be generated in two ways. First, the user terminal 7 when communicating toward the host can send its packets via two or more satellites, **by simply transmitting the same packet towards more than one satellite** from an omni-directional or near omni-directional antenna" (Col. 11, lines 41-46), emphasis added. Therefore Wiedman does not, as applicant argues: "describe a system where each packet is sent once unless a retransmission is requested" (pg 21, lines 5-7).

Applicant further argues: "applicant's system sends the packets a fixed number of times, each duplicate packet having the identical sequence number as the original"

(pg 21, lines10-13). However, Wiedman discloses: "As an example, FIG 15A shows packets arriving at the destination over three different paths. The sender sends four packets 1, 2, 3 and 4 to the destination. There is a TXP time-out associated with these packets. If all the paths are good, **then the destination will receive three packets (for example 1, 1', 1'' as shown in FIG. 15A) for every packet transmitted by the sender. In other words the receiver may receive multiple, duplicate packets**" (Col. 11, lines 59-66), emphasis added. Therefore Wiedman discloses sending the packets a fixed number of times, and each duplicate packet having the identical sequence number as the original.

35. Applicant's arguments, see pgs 21, line 23 – pg 22, line 2, filed 26 March 2008, with respect to the rejection(s) of claim(s) 18 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Baltz, see remarks above.

Conclusion

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW S. LINDSEY whose telephone number is (571)270-3811. The examiner can normally be reached on Mon-Thurs 7:30-5, Fridays 7:30-1.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MSL
5/22/2008

/John Follansbee/

Supervisory Patent Examiner, Art Unit 2151